respectively therefrom and for switching the memory circuit between a first mode of operation and a second mode of operation.

61. (New) A memory circuit, comprising:
control logic for providing an internal mode control signal;
selection and temporary storage circuitry for receiving and storing a first external address; and
a multiplexer coupled to the selection and temporary storage circuitry and to the control logic for receiving the first external address and the internal mode control signal respectively therefrom and for switching the memory circuit between a first mode of operation and a second mode of operation.

62. (New) A memory circuit, comprising:
control logic for providing a mode signal indicating a pipeline or a burst mode;
selection and temporary storage circuitry for receiving and storing a first external address; and
a multiplexer coupled to the selection and temporary storage circuitry and to the control logic for receiving the first external address and the mode signal respectively therefrom and for switching the memory circuit between a burst mode and a pipelined mode.

63. (New) A memory circuit, comprising:
control logic for providing a selected mode control signal;
selection and temporary storage circuitry for receiving and storing a first and a second external address;
a first multiplexer coupled to the selection and temporary storage circuitry and to the control logic for receiving the first external address and the selected mode control signal respectively therefrom;
a second multiplexer coupled to the selection and temporary storage circuitry and to the control logic for receiving the second external address and the selected mode control signal respectively therefrom;

wherein each multiplexer selects its respective external address when the selected mode control signal indicates a pipeline mode, and each multiplexer selects a supplied internal address when the selected mode control signal indicates a pipelined mode.

64. (New) The memory circuit of claim 63, and further comprising:
a counter connected between the control logic and the first and second multiplexers, and operatively connected to receive the first and second external address signals, the counter generating a count 0 and a count 1 signal supplied to the first and second multiplexers, respectively, wherein the count 0 and count 1 signals are selected by the first and second multiplexers when the selected mode control signal indicates a burst mode.

65. (New) A memory circuit, comprising:
control logic for providing a mode signal indicating a pipelined mode or a burst mode of operation;
selection and temporary storage circuitry for receiving and storing a first and a second external address;
a counter connected to the control logic, and coupled to receive the first and the second external address, the counter generating count 0 and count 1 signals; and
a pair of multiplexers, each multiplexer coupled to the selection and temporary storage circuitry, to the counter, and to the control logic, the first multiplexer for receiving the first external address, the count 0 signal, and the selected mode control signal respectively therefrom, and the second multiplexer for receiving the second external address, the count 1 signal, and the selected mode control signal respectively therefrom, the multiplexers selecting the count 0 and count 1 signals when the mode control signal indicates a burst mode, and selecting the first and second external address signals when the mode control circuitry indicates a pipelined mode.

REMARKS

Claims 59-65 are added. As a result, claims 22-32 and 59-65 are now pending in this application.